Cryst. Res. Technol. **38**, No. 11, 968 – 973 (2003) / **DOI** 10.1002/crat.200310122

# Poole-Frenkel electrical conduction in europium oxide films deposited on Si(100)

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Received 4 February 2003, accepted 20 May 2003
Published online 15 October 2003

**Key words** insulating films, europium oxide, dielectric phenomena, metal-oxide-semiconductor (MOS) structures, Poole-Frenkel mechanism.
**PACS** 77.55.+f, 72.20.-I, 73.40.QV

Thin $Eu_2O_3$ films were prepared on Si (P) substrates to form MOS devices. The oxide crystal structure was determined by X-ray diffraction (XRD). The electrical transport properties of the devices with amorphous and crystalline Eu oxide were investigated. The current-voltage and current-temperature characteristics suggest a Poole-Frenkel (PF) type mechanism of carrier transport through the device when the applied field is more than 105 V/cm. A deviation from PF leakage current course was found and attributed to the current carrier trapping. We have also observed that, the dielectric spectra of MOS structure are different when the insulator is an amorphous or crystalline thin film. From which we calculate the relaxation time (τ) of the interface (insulator/semiconductor) dipoles.

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## 1 Introduction

Rare earth oxides (REO) have the most of the fundamental requirements for the alternative gate dielectric in order to achieve performance comparable to $SiO_2$. Among those requirements are bandgap, dielectric constant, high recrystallisation temperature, thermodynamic stability in contact with silicon at temperature exceeding 800 ºC, high quality interface with Si with low interfacial state density $D_{it}$ and lower leakage conduction than $SiO_2$ at an equivalent oxide thickness [1]. REO have high resistivity ($\rho = 10^{12} - 10^{15}$ Ω.cm), high dielectric constant ($\varepsilon$ = 7-20 ) and large band gap ( $E_g$ = 4 –6 eV.) [2]. Moreover, REO are thermodynamically stable in contact with Si substrate, what resists the formation of silicates during the preparation in high vacuum and during annealing in $N_2$ atmosphere. But annealing in oxygen atmosphere can produce a silicate layer due to Si atoms diffusion from substrate into the REO [3,4]. There is also another problem when dealing with REO is the hygroscopic nature of these types of oxides, leading to hydroxide formation after exposure of a thin film to atmospheric conditions.

In this paper, we examine the mechanisms, which control carrier transport in $Al/Eu_2O_3/Si$ structure. This includes the study of temperature, gate voltage and annealing temperature dependence of device leakage current. Also we study the effect of insulator/ semiconductor (I/S) interface charges by dielectric spectroscopy (DS) method.

In spite of numerous study of REO as an insulator in MOS structure [1-12], the study of characteristics and growth of $Eu_2O_3$ on Si substrate is very few [13,14].

## 2 Experimental

Samples of MOS capacitors were manufactured from $Eu_2O_3$ insulator on (100) oriented p-type Si substrates of resistivity between 0.5 and 3.0 Ω.cm. The substrates were thermo-chemically cleaned with 50% potassium

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hydroxide (by weight) solution at 65°C for 15 min. Before the deposition of the oxide layer, heating at about 150°C for 3h in vacuum of $10^{-4}$ Pa degassed the Si substrates. The $Eu_2O_3$ oxide layers were deposited at rate of 0.2 nm/s in vacuum system with pure residual oxygen atmosphere of pressure $1.3x10^{-2}$ Pa on Si substrates held at room temperature. Thickness monitor monitored film thickness.

The as-grown MOS samples were divided into two groups. The first group was annealed in air at 300 ºC for 3h (named as Am300 samples) and the second- at 800°C for 3h (named as Cr800 samples). After annealing, aluminium gate film of around 150 nm was deposited to complete the Al/$Eu_2O_3$/Si (p) structure.

The crystal structure was studied with Philips PW 1710 X-ray diffractometer that using Cu $K_\alpha$ radiation. The ac measurements in frequency range ($10^2$ – $10^6$ Hz) were performed with hp multi- frequency LCR meter with signal amplitude of 50 mV. The dc measurements were done using the standard technique and instruments. Measurements were done in temperature-controlled furnace.

## 3 Structural characterisation of the samples

The reference X-ray diffraction of constituent $Eu_2O_3$ powder shows a C-type, cubic structure of a = 1.086 nm, near from published data [15]. Films annealed at 300 ºC for 3h (Am300) were amorphous while those films annealed at 800 ºC for 3h (Cr800) were crystalline and have [222] orientation, as seen in fig.1. The average grain size of Cr800 sample was calculated by Scherrer formula from the most intense (222) line, to be about 35 nm. It is important to mention here that, the C-phase of $Eu_2O_3$ is stable for temperatures less than 900 ºC; and above this temperature the conversion to the B-phase is possible [16].

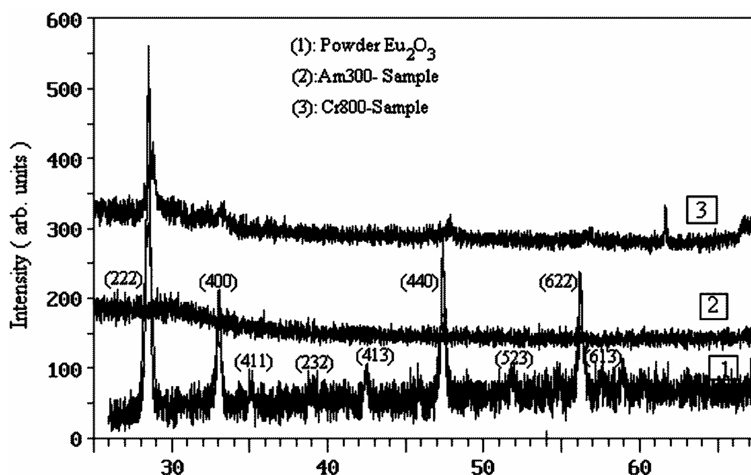


**Fig. 1** X-ray diffraction pattern from the constituent powder ($Eu_2O_3$), amorphous Am300 film and polycrystalline Cr800 film. The scan speed was 0.01 °/s.

## 4 Results and discussion

### 4.1 Dielectric relaxation of the samples

To characterise the dielectric of the samples, we establish the change of the dielectric dynamic response of the prepared MOS-capacitors with an amorphous and polycrystalline $Eu_2O_3$ insulator. Figures 2a and 2b give the frequency dependence at 295 K for the complex-valued capacitance (i.e. the real part C' and the imaginary part C'') of MOS samples with amorphous and crystalline oxide. C''(f) has a typical shape that for polar dielectrics in both structures. Each dependence has unique peak at frequency $f_P$ over the used measurement window; the frequency $f_P = 8.7x10^4$ Hz for the amorphous film and at $f_P = 6.8x10^3$ Hz for the polycrystalline film. C' (f) function of the crystalline sample is nearly constant in the frequency region of $f < f_P$ , while that of the amorphous sample is significantly dispersive This reflects the relatively larger density of captured charged in the amorphous oxide film. A large dispersion of C' (f) is observed at frequencies in the vicinity of peak frequency $f_P$.

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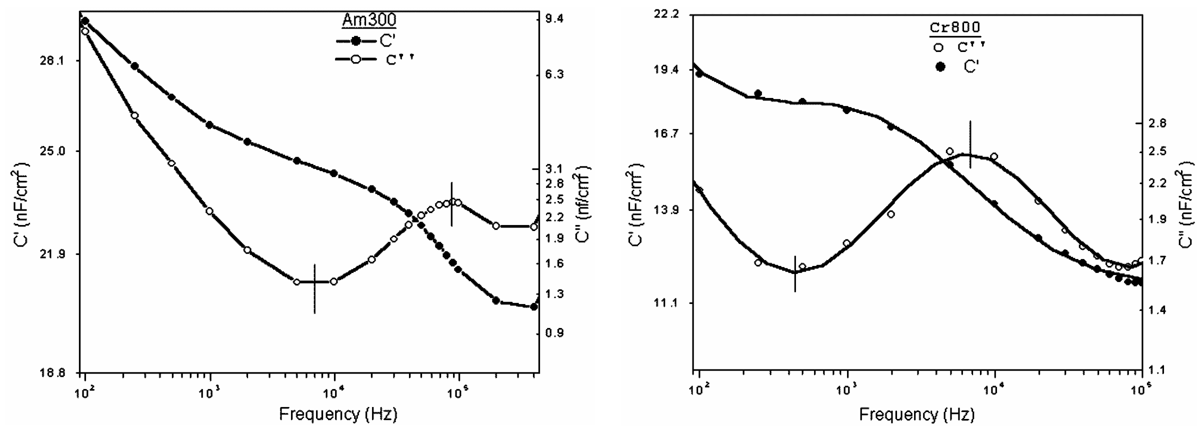


**Fig. 2** The signal frequency dependence of the calculated real C' and imaginary part C'' of the complex capacitance at room temperature (a) for Am300 sample of amorphous $Eu_2O_3$ film and (b) for Cr800 sample of polycrystalline $Eu_2O_3$ film.

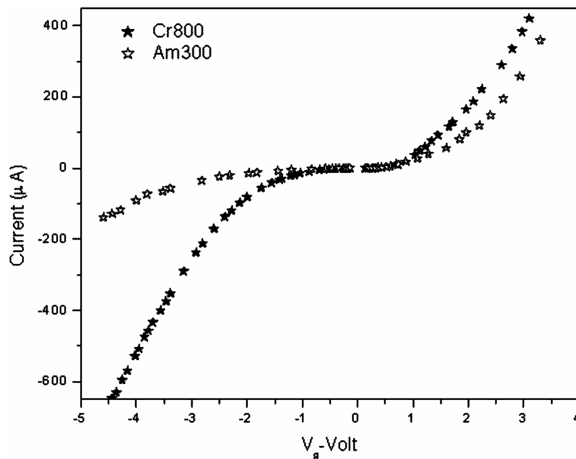


**Fig. 3** Forward and reverse bias characteristic of the sample Am300 and Cr800.

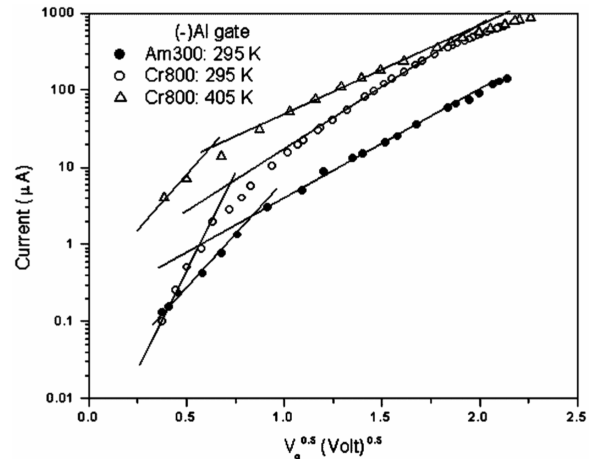


**Fig. 4** Leakage current vs. $V_g^{0.5}$ for Am300 sample at 295 K and for Cr800 at 295K and 405 K. The deviation from PF mechanism begins at current of about 400 µA.

The calculated values of the relaxation time (τ) of the dipoles are $1.2 \times 10^{-5}$ s and $1.5 \times 10^{-4}$ s for amorphous and crystalline films, respectively. We must mention here that, these results point out that the studied dielectric loss peak is an interface (insulator / semiconductor or I/S) type peak so that the results are far from the bulk dipolar relaxation [17]. Therefore, the dielectric spectrum method is sensitive to the variation in the state of the I/S interface that interns depends on the morphological structure of the insulator film in MOS structure. It is seen from fig. 2 that, when the insulator anneals and hence crystallises, the peak of C'' is shifted towards the low frequency by amount of about 6.56 kHz. This shift is due to increasing of I/S interface state $D_{it}$ density. Hence, from $D_{it}$ point of view [1,3], the using of amorphous $Eu_2O_3$ in fabrication of MOS devices is favourable.

## 4.2 DC conduction

Conduction in MOS devices is controlled by several mechanisms. These are, mainly, Schottky emission, Poole-Frenkel emission, Fowler-Nordheim tunnelling, Space charge limited current and ohmic behaviour [18].

Fig. 3 presents the leakage current vs. gate voltage ($I$-$V_g$) curve for Am300 and Cr800 samples at 295 K. The rectification coefficient at bias voltage of magnitude 1.5 V was 5.7 and 2.2 for structures with amorphous and crystalline oxide, respectively. This coefficient is slightly increases with temperature to about 2.7 for the structure with crystalline oxide at 405 K.

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Fig. 4 presents the current-voltage characteristics of Am300 and Cr800 samples at 295 K and for Cr800 at 405 K in negative bias regime.

**MOS structure with amorphous oxide** The behaviour of the characteristics has two regions. In the low field region where field $E < 10^5$ V/cm, the current is due to thermally generated carriers. While the higher field region comply with either Poole-Frenkel or Schottky conduction mechanism. Therefore, the results can be described by eqn.(1):

$$J = A^* T^2 \exp \{ e ( \beta_{Sc} E^{1/2} - \Phi_{Sc} ) / k_B T \} \quad (1)$$

for Schottky effect, and by eqn.(2):

$$J = J_o \exp \{ e (\beta_{PF} E^{1/2} - \Phi_{PF} ) / k_B T \} \quad (2)$$

for Poole-Frenkel effect [18].

Where $A^*$ is the effective Richardson constant, $\Phi$ is the barrier height for each mechanism and $J_o$ ($J_o \sim E$) is the low- field current density. Schottky $\beta_{Sc}$ and Poole-Frenkel $\beta_{PF}$ field lowering coefficients are given by:

$$2\beta_{Sc} = \beta_{PF} = (e^3 / \pi \varepsilon_o \varepsilon_{ox} )^{1/2} \quad (3)$$

Where $\varepsilon_{ox}$ is the static dielectric constant of the insulator and other symbols have their usual meanings. If we consider the static value $\varepsilon_{ox} = 13.9$ [19], then the theoretical values of these coefficients are $\beta_{Sc} = 1.02 \times 10^{-5}$ eV.m$^{1/2}$.V$^{-1/2}$ and $\beta_{PF} = 2.03 \times 10^{-5}$ eV.m$^{1/2}$.V$^{-1/2}$. But the experimental value of $\beta$ as determined from the high-field part of the plot in fig.4 for Am300 is $2.4 \times 10^{-5}$ eV.m$^{1/2}$.V$^{-1/2}$. Hence, the experimental value of $\beta$ is closer to the calculated $\beta_{PF}$ value. This suggests that the dominant conduction mechanism in the studied structure is Poole-Frenkel (PF) type. This is indeed an expected result since; the high density of structural defects in thin films cause additional energy states close to the band edge –traps. These traps restrict the current flow because of a capture and emission process, thereby becoming the dominant current mechanism.

The value of $\beta$ as determined from the low-field region of fig.4 for Am300 is $4.6 \times 10^{-5}$ eV.m$^{1/2}$.V$^{-1/2}$, which is far to be consistent with the theoretical values of $\beta_{Sc}$ or $\beta_{PF}$. Therefore, this region is due to thermally activated conductivity mechanism with thermal activation energy of 0.13 eV. Moreover, if we plot $\ln(J/T^2)$ vs. $T^{-1}$ for $V_g = -0.78$ V by assuming that it obeys Schottky mechanism we get small and unacceptable value of $A^*$ ($A^* = 7.3 \times 10^{-5}$ A/m$^2$.K).

In addition, the relationship between Log (I) vs. $T^{-1}$ for gate voltages of –0.78 V and –1.95 V are linear as shown in fig.5. There, we notice two distinct temperature regions; lower and above about 373 K. This transition is more likely related to the hygroscopic nature of $Eu_2O_3$. We can postulate that humidity incorporation in the film is in a form of hydroxyl OH, as mentioned by [20] for $Gd_2O_3$ and by [3] for $Y_2O_3$ and $Gd_2O_3$. We notice that the change of the slope of fig.5 appears only for curve in the Poole-Frenkel region (at $V_g$ =-1.95 V) where the conduction mechanism is limited by oxide bulk. Meanwhile, the conduction mechanism in the lower voltage region ($V_g$ = -0.78 V-graph) which is mainly controlled by the Al/$Eu_2O_3$ interface, has no change of slope. The calculated value of PF barrier height $\Phi_{PF}$ is 0.34 eV in low-temperature region and 0.19 eV in high-temperature region

**MOS structure with crystalline oxide** From fig.4 we observe three field regions. The low field region $E < 10^5$ V/cm is also attributed to thermally generated carriers. The middle field region of E is larger than about $10^5$ V/cm and less than about $3 \times 10^5$ V/cm is the result of Poole-Frenkel conduction mechanism. The current flow through the structure depends highly on temperature at low biases. But, it reaches a regime of third region, at fields around $3 \times 10^5$ V/cm, where the current increases slowly with the applied voltage and becomes almost independent of temperature. The “quasi-saturation” of the current is may be caused by the charge trapping [21]. Consequently, an internal electric field is created, which is opposed to the external electric field, limiting the carriers’ flow [22].

In the middle region before the quasi saturation occurs, the current can be fitted with a Poole-Frenkel current eqn.(2) with $\beta_{PF} = (e^3 / \pi \varepsilon_o \varepsilon )^{1/2}$, where $\varepsilon$ is considered to be the effective static dielectric constant of

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the multilayer insulator between Al-gate and Si-wafer. It is reasonable to assume that an amorphous $SiO_2$ thin layer and amorphous silicate layer (Eu-Si-O) are formed during the annealing in air at 800°C. The silicate layer is formed as a result of Si diffusion in the Eu oxide layer. Such model was discovered experimentally with $Gd_2O_3$ and $Y_2O_3$ [3,11] by using medium energy ion scattering (MEIS) and scanning transmission electron microscopy (STEM). The silicate layer was also observed by using MEIS measurements and showed that yttria film annealed at 700°C resulted in Si uptake from the substrate into $Y_2O_3$, and formation of silicate layer extending to about 1.5 nm in width [23]. Also, It was observed an $SiO_2$ layer sandwiched between Si and $Y_2O_3$ [10], Si and $Er_2O_3$ [5] of thickness 1-2.5 nm. The PF current was found to fit the measurements. By using the same experimental β-value of Am300 ($2.4\times10^{-5}$ $eV.m^{1/2}.V^{-1/2}$) we calculate ε to be 6.0. This low value of effective dielectric constant is due to reduced dielectric constant of formed silicate layer. We can estimate the formed amorphous silicate layer thickness to be 6 nm at least.

As we see from Fig.5, crystalline sample Cr800 is not sensitive to the hygroscopic nature of the oxide. The calculated average value of PF barrier height $\Phi_{PF}$ is 0.18 eV.

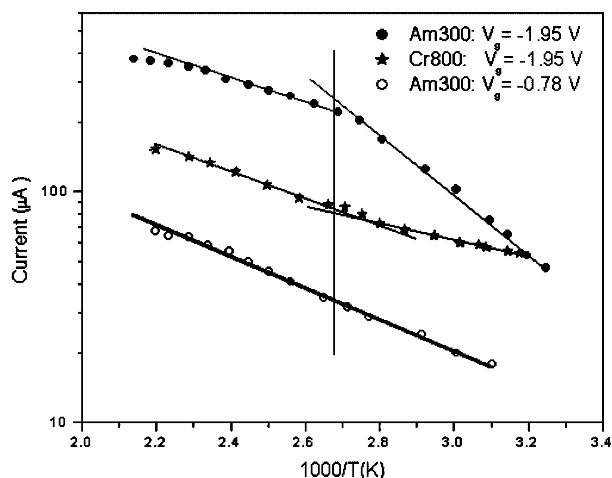


**Fig. 5** Arrhenius plot of temperature dependent of leakage current for Am300 MOS device at bias Voltages: Vg = -0.78 V and Vg = 1.95 V, and for Cr800 at Vg = -1.95 V.

## 5 Conclusion

We have investigated the electrical transport properties of $Al/Eu_2O_3/Si(P)$ devices with amorphous and crystalline Eu oxide. The current-voltage and current-temperature characteristics suggest a PF type mechanism of carrier transport through the device when the applied gate field is more than $10^5$ V/cm. The value of $\Phi_{PF}$ is 0.34 eV and 0.19 eV for the device of amorphous Eu oxide in low-temperature region (i.e. for temperature less than about 373 K) and in high-temperature region, respectively. For the device of crystalline Eu oxide $\Phi_{PF}$ is about 0.18 eV and is almost independent of temperature. It was observed a deviation from PF behaviour towards current quasi saturation state when the current in the device becomes more than about 400 μA or at fields more than about $-3\times10^5$ V/cm. We used the dielectric spectroscopy method to determine the relaxation time (τ) of the interface I/S dipoles to be $1.2\times10^{-5}$ s and $1.5\times10^{-4}$ s for amorphous and crystalline films, respectively. The shift of the C''(f) peak is related to the density of interface states $N_{it}$.

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